NEC
ELECTRON DEVICE

MOS DIGITAL INTEGRATED CIRCUIT
μPD6300C

LATCH and DRIVER for FIP
CMOS LSI

DESCRIPTION

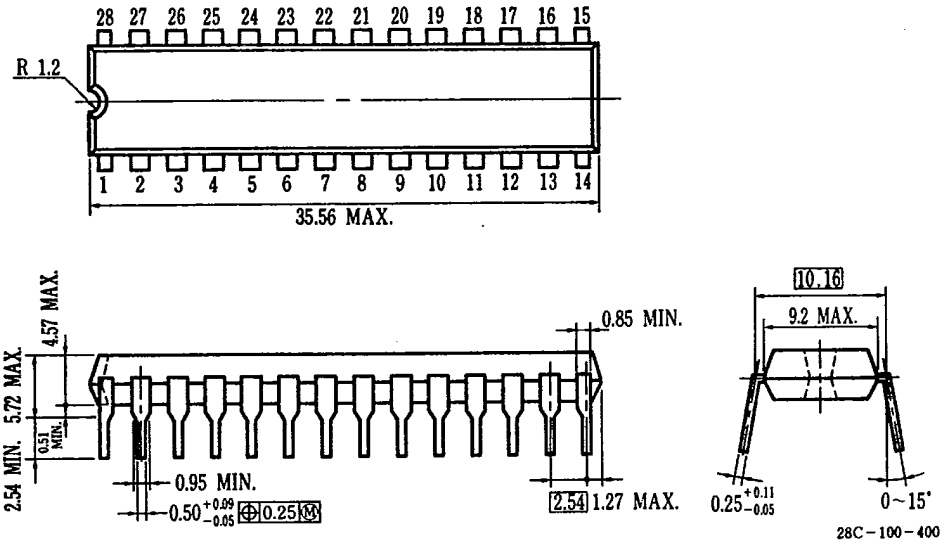
The μPD6300C is a latch and driver CMOS IC for FIP (Fluorescent Indicator Panel). For multiplex wiring, the μPD6300C is supplied with the serial interface circuit, 20 bit shift register, 20 bit data latch and 20 bit drivers. The serial data transfer from the data source to the μPD6300C is accomplished with 3 or 4 signals.

FEATURES

- Serial Input 20 bit Sift Register Incorporated.
- 20 bit Output Data Latch Incorporated.
- 20 bit Output Drivers for FIP.
- Output Characteristics V_{out} = 40 V.
  I_{out} = 5 mA.
- Serial Interface Format: Compatible with NEC microcomputer.
- Brightness Control Enable: External Duty Control.
- Wide Operating Temperature Range T_{opt} = –40 to +85 °C.
- 28 PIN Plastic Molded Slim DIP (Dual In line Package).

PACKAGE DIMENSIONS (Unit: mm)

28PIN PLASTIC DIP(400mil)



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage at V_{DD} terminal	V_{DD}	−0.3 to +7.0 *1	V
Input Voltage	V_{IN}	−0.3 to V_{DD} *1	V
Output Voltage (1~7, 15~27 Pins)	V_{O0} to V_{O19}	−35 *1, *2	V
Output Current (1~7, 15~27 Pins)	I_{O0} to I_{O19}	−5	mA
Operating Temperature Range	T_{opt}	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Notes: *1; These Voltage are referenced to the V_{SS}.
*2; V_{DD} = 5 V

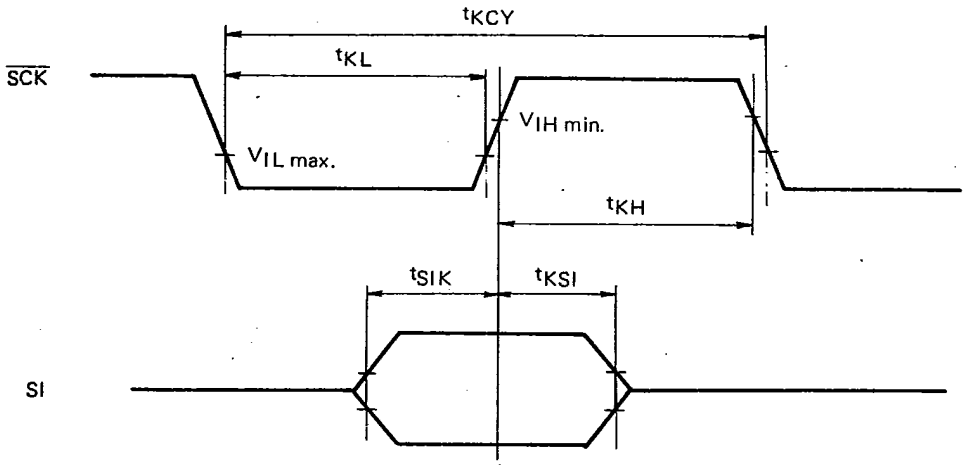
RECOMMENDED OPERATING CONDITIONS

	CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
	Operating Temperature Range	T_{opt}	−40		+85	°C
	Operating Supply Voltage	V_{DD}	4.5	5.0	5.5	V
*3	Output Voltage (1~7, 15~27 Pins)	V_{O0} to V_{O19}		−22	−35	V
	Output Current (1~7, 15~27 Pins)	I_{O0} to I_{O19}		−2.0	−5.0	mA
	Input Voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V
	Input Voltage Low	V_{IL}	V_{SS}		0.3 V_{DD}	V
	$\overline{SCK}$ Frequency	$f_{\overline{SCK}}$			500	kHz
*4	$\overline{SCK}$ Cycle Time	t_{KCY}	2.0			μs
*4	$\overline{SCK}$ High Level Pulse Width	t_{KH}	0.9			μs
*4	$\overline{SCK}$ Low Level Pulse Width	t_{KL}	0.9			μs
*4	SI Setup Time to $\overline{SCK}$↑	t_{SIK}	0.4			μs
*4	SI Hold Time	t_{KSI}	0.4			μs
*5	$\overline{CS}$↓−$\overline{SCK}$↓ Valid Time	t_{CSL}	0			μs
*5	$\overline{CS}$↓−$\overline{SCK}$↑ Valid Time	t_{CSH}	0.9			μs
*5	$\overline{SCK}$ −LH↓ Valid Time	t_{SKL}	0			μs
*5	LH Low Level Pulse Width	t_{LL}	1.8			μs
*5	LH↑−$\overline{CS}$↑ Valid Time	t_{LHC}	0.9			μs
*6	LH Delay Time	t_{LHD}			1.9	μs

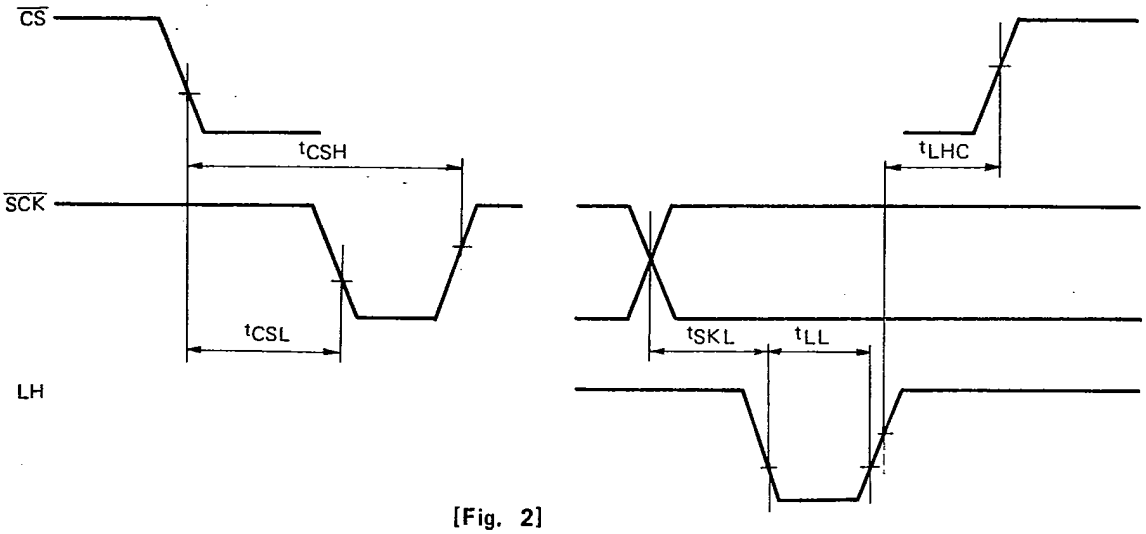
Notes: *3; These Voltage are referenced to the V_{DD}.
*4; See Fig. 1
*5; See Fig. 2
*6; See Fig. 3

ELECTRICAL CHARACTERISTICS (Recommended Operating Conditions)

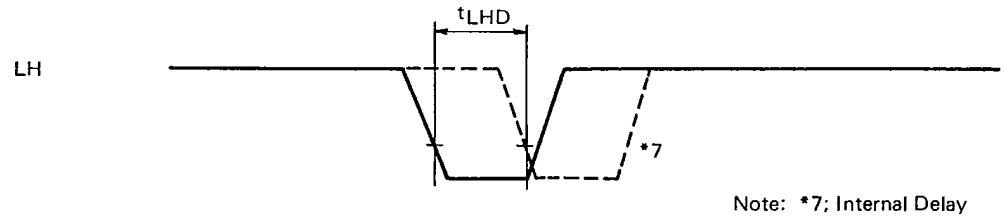
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Leakage Current	I_{IL}			±10	μA	$V_{IN}=V_{SS}$ or V_{DD}
SO Output Voltage High	V_{SOH}	$V_{DD}-1$			V	$I_{SOH}=-1$ mA
SO Output Voltage Low	V_{SOL}			0.4	V	$I_{SOL}=0.8$ mA
Output Voltage High (1~7, 15~27 Pins)	V_O	$V_{DD}-15$			V	$I_O=-5$ mA O_0 to O_{19} Output
Output Leakage Current (1~7,15~27 Pins)	I_{OLL1}			1.0	μA	$V_O=-10$ V
	I_{OLL2}			10.0	μA	$V_O=-20$ V
Supply Current at V_{DD} Terminal	I_{DD}			1	mA	$V_{DD}=5.5$ V All Input = [High] All Output = Open
$\overline{SCK}$↓ – SO Valid Time	t_{KSO}			0.5	μs	See Fig. 4
Input Capacitance	C_{IN}			15	pF	f=1 MHz



[Fig. 1]

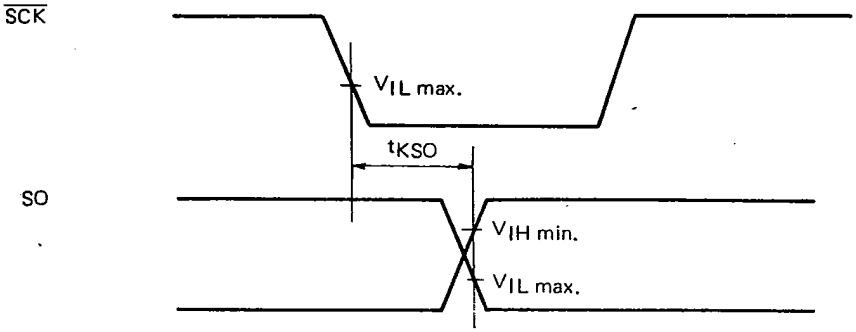


[Fig. 2]



Note: *7; Internal Delay

[Fig. 3]



[Fig. 4]

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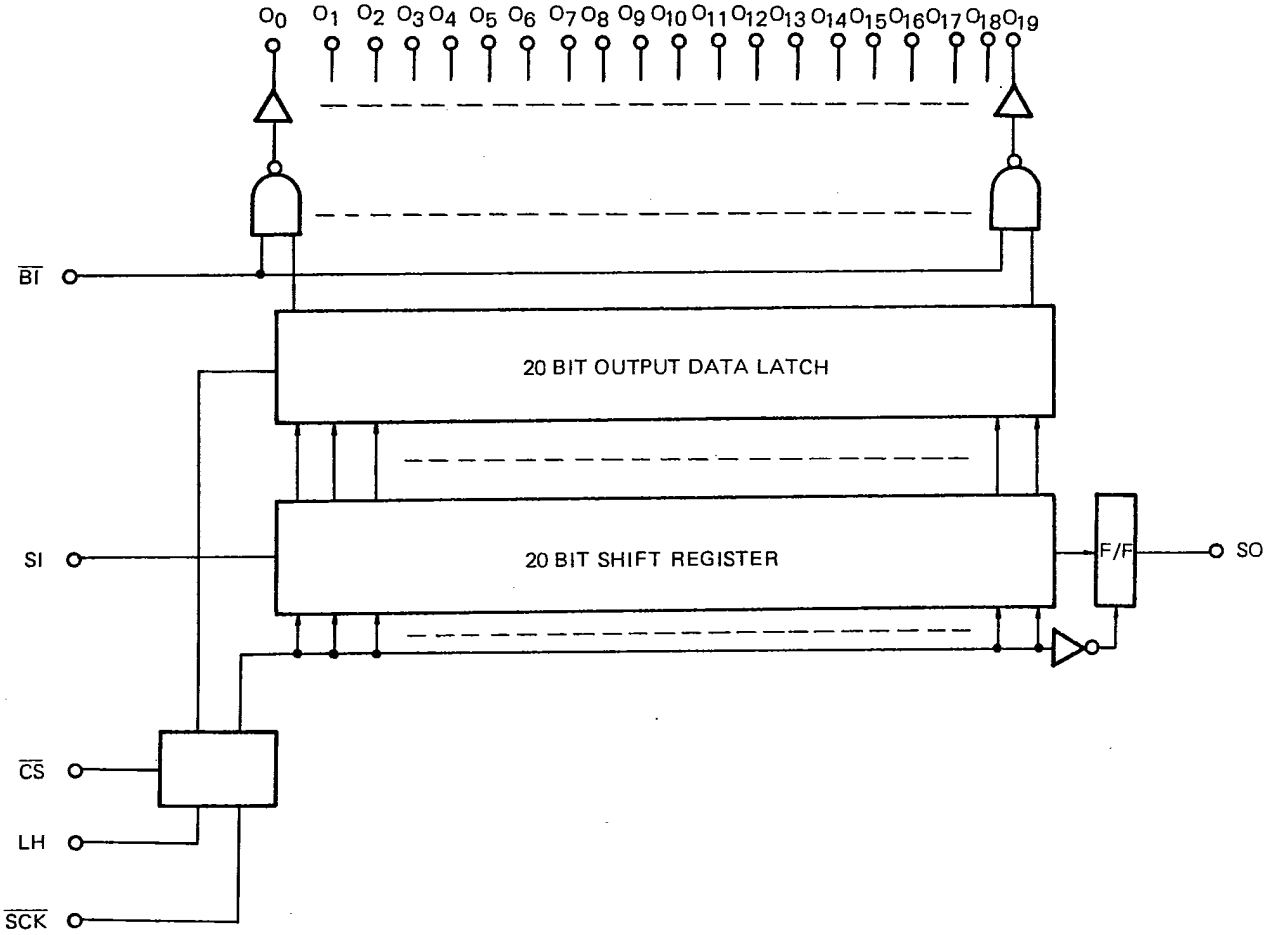
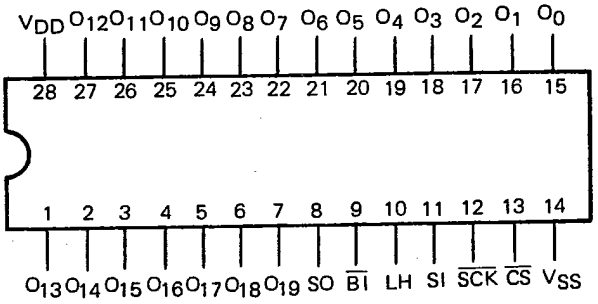
BLOCK DIAGRAM



PIN CONNECTION (Top View)



FUNCTION

$O_0 \sim O_{19}$: Output, P ch MOS Open Drain
These 20 Outputs are the Outputs of 20 bit output data latch and can drive FIP directly.

$\overline{BI}$: Blanking Input
When "L" level signal is supplied to the BI, O_0 to O_{19} are disable.
"H" : O_0 to O_{19} are active.

LH : Latch and Hold Input
When "L" level signal is supplied to the LH,
The data of 20 bit shift register are normally transfered the 20 bit output data latch.
At the time of the rising edge of LH; the data of 20 bit output data latch are hold.
"H" ; The data of 20 bit output data latch are protected.

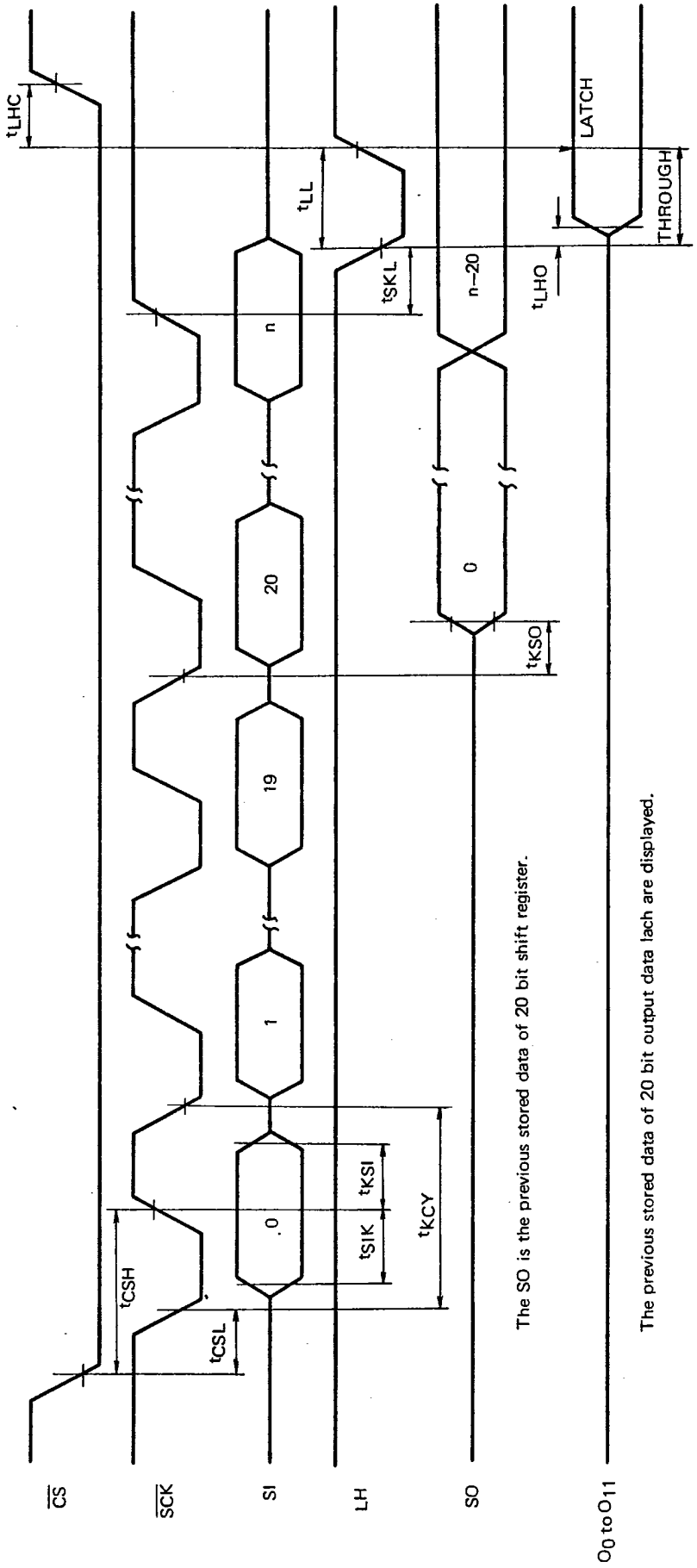
SI : Serial Data Input

$\overline{SCK}$: Serial Clock Input
The SI data are read and stored in the 20 bit shift register at the rising edge of $\overline{SCK}$.

SO : Serial Data Output. CMOS push-pull
The SO is a signal of serial output data from 20 bit sift register.

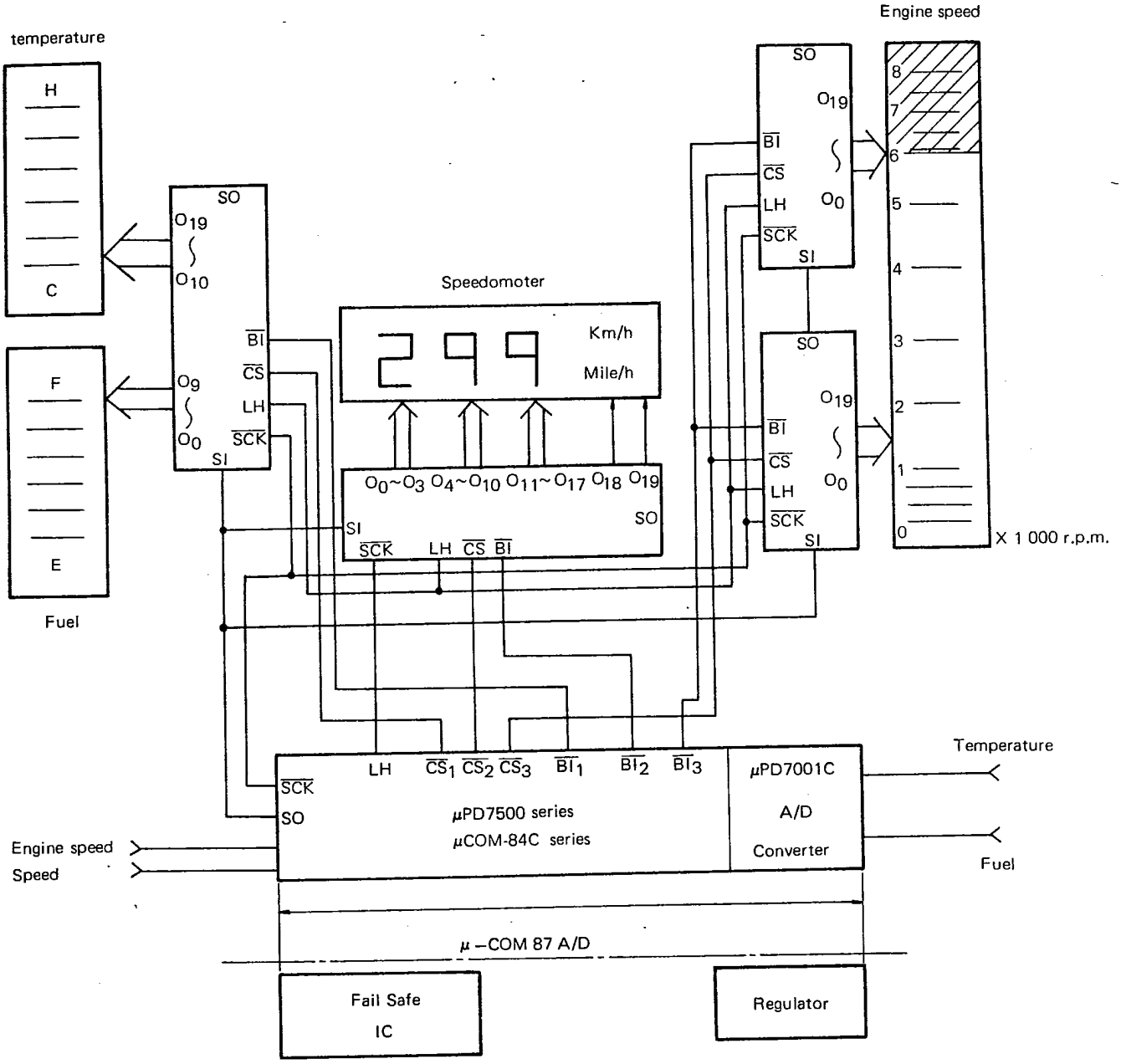
$\overline{CS}$: Chip Select Input
When the CS is "L" level, the LH and $\overline{SCK}$ are active.

TIMING CHART



APPLICATION CIRCUIT

AUTOMOTIVE DASHBOARD SYSTEM

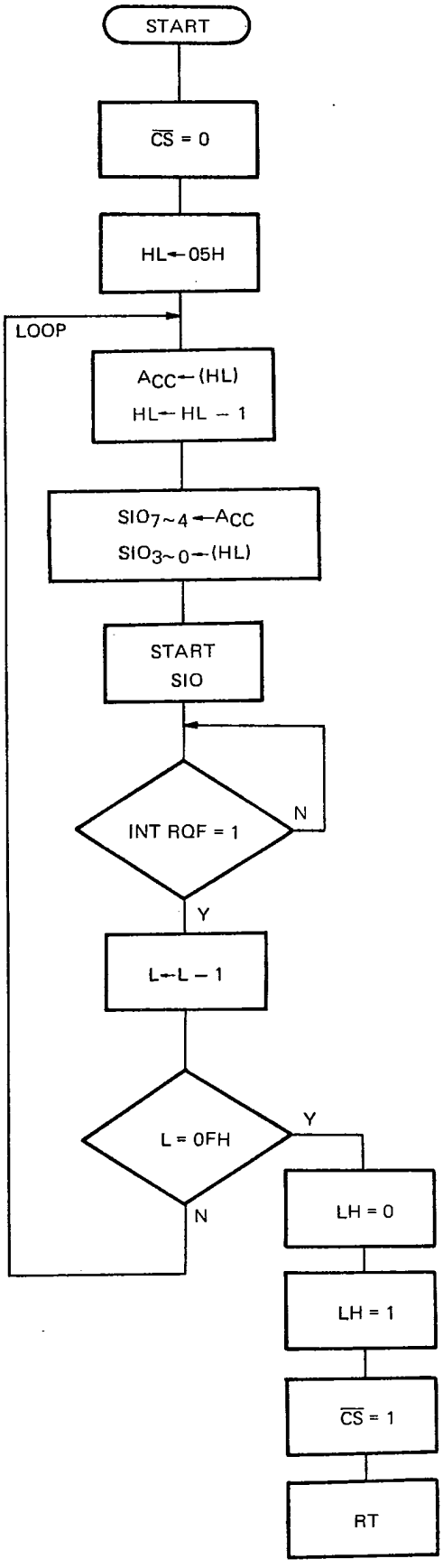


EXAMPLE OF SOFTWARE

Using of serial I/O of μ-COM75 series

Subroutine of 24 bit data transfer

```
SI OUT  :  ANP  6, 0BH
        :  LHLI 05H
LOOP    :  LAM  HL-
           TAMSIO
           SIO
           SKI  2
           JCP  $-2
           DLS
           JCP  LOOP
           ANP  6, 7
           ORP  6, 8
           ORP  6, 4
           RT
```



RAM (ADD)				
	3	2	1	0
00H	O_3	O_2	O_1	O_0
01H	O_7	O_6	O_5	O_4
02H	O_{11}	O_{10}	O_9	O_8
03H	O_{15}	O_{14}	O_{13}	O_{12}
04H	O_{19}	O_{18}	O_{17}	O_{16}
05H	O_{23}	O_{22}	O_{21}	O_{20}

P_{62} – $\overline{CS}$

P_{63} – LH